AMENDMENTS TO THE CLAIMS

The claims and their status are reflected below. Claims 1-39, 52-77 are pending in the application prior to any amendments below.

1. (Previously presented) A method for programming a memory system, said system comprising strings of charge storage transistors for storing different charge states, each of said strings including two select transistors, each of said strings connected between one of a plurality of bit lines and a source line, said strings controlled by a common set of word lines, wherein at least a first transistor in a first string of the strings and adjacent to one of the two select transistors in the first string is in a desired charge storage state, said method comprising:

applying a program voltage level through one of the word lines to a control gate that is capacitively coupled with a second transistor in a second string of the strings different from the first string to program the second transistor, said second transistor separated from the source line or the bit line connected to the second string by three or more charge storage transistors in said second string; and

boosting through some of the word lines electrical potential(s) of channel regions of the first string of transistors by coupling voltage levels to at least some of the transistors in the first string to reduce program disturb, wherein the electrical potential(s) of the channel regions of some of the transistors in the first string are/is boosted so that breakdown at the drain or source side of the one select transistor in the first string is reduced to such an extent that it does not result in a change of the first transistor's desired charge storage state to a different charge state.

2. (Currently amended) The method of claim 1, wherein said coupling couples a first voltage to the first transistor and a second ~~boosting~~ voltage to at least some of the remaining transistors in the first string, the second voltage being higher than the first voltage.

3. (Original) The method of claim 2, the second voltage being higher than the first voltage by at least 50% of the first voltage.

4. (Original) The method of claim 1, wherein the electrical potential(s) of the channel regions of some of the transistors in the first string are/is boosted so that band-to-band tunneling at the drain or source side of the one select transistor is reduced to such an extent that it does not result in a change of the first transistor's desired charge storage state to a different charge state.

5. (Original) The method of claim 4, wherein said band-to-band tunneling at the drain side of the source select transistor is suppressed.

6. (Original) The method of claim 2, wherein said first voltage is in a range of about 1 to 3 volts.

7. (Original) The method of claim 2, wherein said second voltage is in a range of about 5 to 10 volts.

8. (Previously presented) The method of claim 2, further comprising coupling a third voltage to the one select transistor in the first string to cause it to be electrically non-conducting, and wherein the first voltage is higher than the third voltage.

9. (Original) The method of claim 1, wherein the control gate also controls a third charge storage transistor in the first string, said method further comprising turning off at least a fourth charge storage transistor in the first string between the source line and the third transistor, in order to electrically isolate the third transistor from transistors in the first string between the source line and the fourth transistor.

10. (Original) The method of claim 9, further comprising turning off at least a fifth charge storage transistor in the first string between the bit line connected to the first

string and the third transistor, in order to electrically isolate the third transistor from transistors in the first string between such bit line and the fifth transistor.

11. (Original) The method of claim 10, wherein each of the fourth and fifth transistors are separated from the third transistor by at least one transistor in the first string.

12. (Original) The method of claim 9, wherein the fourth transistor is separated from the third transistor by at least one transistor in the first string.

13. (Previously presented) A method for programming a memory system, said system comprising strings of charge storage transistors for storing different charge states, each of said strings including two select transistors, said strings controlled by a common set of word lines and connected between a plurality of bit lines and a source line, wherein a first transistor in a first string of the strings and adjacent to one of the two select transistors is in a desired charge storage state of more than two possible charge storage states, said method comprising:

applying through one of the word lines a program voltage level to a control gate that is capacitively coupled with a second transistor in a second string of the strings to program the second transistor, said second transistor separated from the source line or the bit line connected to the second string by three or more charge storage transistors in said second string; and

boosting through some of the word lines electrical potential(s) of channel regions of the first string of transistors by coupling voltage levels to at least some of the transistors in the first string to reduce program disturb, wherein the electrical potential(s) of the channel regions of some of the transistors in the first string are/is boosted so that such boosting does not result in a change of the first transistor's desired charge storage state to a different one of the more than two possible charge states.

14. (Currently amended) A method for programming a memory system, said system comprising strings of charge storage transistors for storing different charge states,

said strings including a first string, each of the strings including two select transistors, said strings controlled by a common set of word lines and connected between a plurality of bit lines and a source line, wherein a first charge storage transistor in the first string and adjacent to one of the two select transistors is in a desired charge storage state, said method comprising:

applying a program voltage level to a first control gate that is capacitively coupled with a second charge storage transistor, and subsequently applying a program voltage level to a second control gate that is capacitively coupled with a third charge storage transistor different from the second transistor to program the second and third transistors, each of said second and third transistors being in a second string of the strings different from the first string and being separated from the source line or the bit line connected to the second string by two~~one~~ or more charge storage transistors in said second string; and

boosting electrical potential(s) of channel regions of the first string of transistors by coupling boosting voltage levels to at least some of the transistors and a voltage level to the first transistor in the first string to reduce program disturb, wherein the voltage level coupled to the first transistor is different from that/those coupled to other transistors in the first string when a program voltage level is applied to the control gates coupled to the second and third transistors.

15. (Previously presented) The method of claim 14, said method comprising a plurality of programming time intervals to program all the transistors in the second string, wherein during each of said plurality of programming time intervals a program voltage level is coupled to one of the transistors in said second string to program such transistor, and the voltage level coupled to the first transistor is different from that/those coupled to other transistors in the first string during two or more of said plurality of programming time intervals.

16. (Original) The method of claim 14, wherein the electrical potential(s) of the channel regions of the first string are/is boosted so that breakdown at the drain or source side of the one select transistor is reduced to such an extent that it does not result in a change of the first transistors desired charge storage state to a different charge state.

17. (Original) The method of claim 16, wherein the electrical potential(s) of the channel regions of the first string are/is boosted so that said band-to-band tunneling at the drain or source side of the one select transistor is suppressed.

18. (Previously presented) The method of claim 16, wherein the desired charge storage state is one of more than two possible charge storage states of the first transistor, and said coupling the voltage level to the first transistor does not result in a change of the first transistor's desired charge storage state to a different one of the more than two possible charge states.

19. (Currently amended) The method of claim 14, wherein said coupling couples a first voltage to the first transistor and a second ~~boosting~~ voltage to at least some of the remaining transistors in the first string, the second voltage being higher than the first voltage.

20. (Original) The method of claim 19, the second voltage being higher than the first voltage by at least 50% of the first voltage.

21. (Original) The method of claim 19, wherein said first voltage is in a range of about 1 to 3 volts.

22. (Original) The method of claim 19, wherein said second voltage is in a range of about 5 to 10 volts.

23. (Previously presented) The method of claim 19, further comprising coupling a third voltage to the one select transistor in the first string to cause it to be electrically non-conducting, and wherein the first voltage is higher than the third voltage.

24. (Original) The method of claim 14, wherein the first or second control gate also controls a fourth charge storage transistor in the first string, said method further

comprising turning off at least a fifth charge storage transistor in the first string between the source line and the fourth transistor, in order to electrically isolate the fourth transistor from charge storage transistors in the first string between the source line and the fifth transistor.

25. (Original) The method of claim 24, wherein the fifth transistor is separated from the fourth transistor by at least one transistor in the first string.

26. (Original) The method of claim 24, further comprising turning off at least a sixth charge storage transistor in the first string between the bit line connected to the first string and the fourth transistor, in order to electrically isolate the fourth transistor from charge storage transistors in the first string between such bit line and the sixth transistor.

27. (Original) The method of claim 26, wherein each of the fifth and sixth transistors are separated from the fourth transistor by at least one charge storage transistor in the first string.

28. (Currently amended) A method for programming a memory system, said system comprising strings of charge storage transistors for storing different charge states, said strings including a first and a second string each connected between one of a plurality of bit lines and a source line and controlled by common word lines, said method comprising:

applying a program voltage to a selected word line coupled to a selected transistor in the first string separated from the source line by at least two charge storage transistors in the first string to program the selected transistor;

coupling first ~~boosting~~ voltage level(s) to all of the transistors in the second string between said selected word line and the bit line connected to the second string to boost electrical potential(s) of channel regions of transistors in the second string to a value or values closer to the program voltage to reduce program disturb; and

coupling second voltage level(s) that are or is less than the first voltage level(s) to at least two adjacent charge storage transistors in the second string between the selected word line and the source line, said second voltage level(s) being such that a channel area of the second string on the source side of the at least two adjacent transistors is electrically isolated from the transistor in the second string controlled by the selected word line to reduce program disturb, said second voltage level(s) including a voltage level at or about 0 volts and a positive voltage level.

29. (Previously presented) The method of claim 28, wherein the second voltage level(s) coupled to at least one of the at least two adjacent transistors in the second string turns off such at least one transistor.

30. (Previously presented) The method of claim 29, wherein the second voltage level(s) coupled to the at least two adjacent transistors is such that the at least one transistor that is turned off is separated from the selected word line by at least one charge storage transistor in the second string.

31. (Original) The method of claim 30, wherein a positive voltage is coupled to said at least one transistor in the second string separating the selected word line from the transistor that is turned off.

32. (Currently amended) The method of claim 31, wherein said positive voltage is in a range of about 1 to 32 volts.

33. (Previously presented) The method of claim 31, wherein the second voltage levels include a positive voltage coupled to at least one transistor in the second string adjacent to but separated from the selected word line by the at least two adjacent transistors.

34. (Cancelled)

35. (Previously presented) The method of claim 28, wherein the second string includes two select transistors, wherein a first transistor in the second string and immediately adjacent to one of the two select transistors is in a desired charge storage state, further comprising coupling a third voltage level to the first transistor in the desired charge storage state such that the coupling of the third voltage level and boosting of the electrical potential(s) of the channel regions of the second string do not change the desired charge storage state of the first transistor to a different charge state.

36. (Original) The method of claim 35, wherein breakdown at the drain or source side of the one select transistor as a result of the third voltage level and boosting of the electrical potential(s) of the channel regions of the second string is reduced to such an extent that it does not result in a change of the first transistor's desired charge storage state to a different charge state.

37. (Original) The method of claim 35, wherein the desired charge storage state is one of more than two possible charge storage states of the first transistor, and said coupling the third voltage level to the first transistor does not result in a change of the first transistor's desired charge storage state to a different one of the more than two possible charge states.

38. (Currently amended) The method of claim 28, wherein the second string includes two select transistors, wherein a transistor in the second string and immediately adjacent to one of the two select transistors is in a desired charge storage state, wherein the program voltage is coupled sequentially to at least two selected charge storage transistors in the first string by applying the program voltage to two control gates capacitively coupled with the at least two selected transistors,

coupling a third voltage level to the transistor in the desired charge storage state when the program voltage is applied to the two control gates, such that the coupling of said third voltage level and boosting of the electrical potential(s) of the channel regions of the second string does not change the desired charge storage state to a different charge state, said third voltage level being less than the first ~~boosting~~ voltage level(s).

39. (Currently amended) The method of claim 28, wherein the at least two adjacent transistors in the second string are separated by at least one charge storage transistor to which one of the first ~~boosting~~ voltage level(s) is coupled.

40. - 51. (Cancelled)

52. (Currently amended) A method for programming a memory system, said system comprising strings of charge storage transistors for storing different charge states, said strings including a first and a second string each connected between one of a plurality of bit lines and a source line and controlled by common word lines, said method comprising:

applying a program voltage to a selected word line coupled to a selected transistor in the first string separated from the source line by at least two charge storage transistors in the first string to program the selected transistor;

coupling first ~~boosting~~ voltage level(s) to all of the transistors in the second string between said selected word line and the bit line connected to the second string to boost electrical potential(s) of channel regions of transistors in the second string to a value or values closer to the program voltage to reduce program disturb; and

coupling second voltage level(s) that are or is less than the first voltage level(s) to at least two charge storage transistors in the second string between the selected word line and the source line, said second voltage level(s) being such that a channel area of the second string on the source side of the at least two transistors is electrically isolated from the transistor in the second string controlled by the selected word line to reduce program disturb, said second voltage level(s) including a voltage level at or about 0 volts and a positive voltage level.

53. – 54. (Cancelled).

55. (Previously amended) The method of claim 52, wherein the second voltage level(s) are such that at least one of the at least two transistor is turned off.

56. (Original) The method of claim 55, wherein the at least one transistor that is turned off is separated from the selected word line by at least one charge storage transistor in the second string.

57. (Original) The method of claim 56, wherein a positive voltage is coupled to said at least one transistor in the second string separating the selected word line from the transistor that is turned off.

58. (Currently amended) The method of claim 57, wherein said positive voltage is in a range of about 1 to 32 volts.

59. (Original) The method of claim 52, wherein the at least two charge storage transistors in the second string are adjacent to each other.

60. (Currently amended) A method for programming a memory system, said system comprising strings of charge storage transistors for storing different charge states, said strings including a first and a second string each connected between one of a plurality of bit lines and a source line and controlled by common word lines, said method comprising:

applying a program voltage to a selected word line coupled to a selected transistor in the first string separated from the source line and from the bit line connected to the first string by at least two charge storage transistors in the first string to program the selected transistor;

boosting electrical potential(s) of channel regions of some of the charge storage transistors in the second string of transistors by coupling first ~~boosting~~ voltage level(s) to some of the transistors on drain and source sides of a corresponding transistor in the second string controlled by the selected word line, such corresponding transistor in the second string separated from the source line by at least a first set of at least two charge storage transistors in the first string, and from the bit line connected to the second string by a second set of at least two charge storage transistors in the second string, the two sets located adjacent to the corresponding transistor; and

applying second voltage level(s) that are or is less than the first voltage level(s) to word lines controlling the two sets of adjacent transistors to turn off at least one transistor in each set, to reduce program disturb, wherein the second voltage level(s) contain(s) at least one voltage level such that an unprogrammed transistor in the first string coupled to such at least one voltage level will be turned on but a programmed transistor in the first string coupled to such at least one voltage level will be turned off, said second voltage level(s) applied to the first set of transistors including a voltage level at or about 0 volts and a positive voltage level.

61 - 62. (Cancelled).

63. (Previously presented) The method of claim 60, wherein the second voltage level(s) coupled to the two sets of transistors are such that the at least one transistor that is turned off in each of the two sets is separated from the selected word line by at least one charge storage transistor in the second string.

64. (Original) The method of claim 63, wherein a positive voltage is coupled to said at least one transistor in the second string separating the selected word line from the transistor that is turned off in each of the two sets.

65. (Currently amended) The method of claim 64, wherein said positive voltage is in a range of about 1 to 3~~2~~ volts.

66. (Original) The method of claim 60, wherein different voltage levels are coupled to the adjacent transistors in each of the two sets in the second string.

67. (Original) The method of claim 60, wherein the second string includes two select transistors, wherein a first transistor in the second string and immediately adjacent to one of the select transistors is in a desired charge storage state, further comprising coupling a third voltage level to the first transistor such that coupling of the third voltage level and boosting of the electrical potential(s) of the channel regions of the

second string do not change the desired charge storage state of the first transistor to a different charge state.

68. (Original) The method of claim 67, wherein breakdown at the drain or source side of the one select transistor as a result of the third voltage level and boosting of the electrical potential(s) of the channel regions of the second string is reduced to such an extent that it does not result in a change of the first transistor's desired charge storage state to a different charge state.

69. (Original) The method of claim 67, wherein the desired charge storage state is one of more than two possible charge storage states of the first transistor, and said coupling the third voltage level to the first transistor does not result in a change of the first transistor's desired charge storage state to a different one of the more than two possible charge states.

70. (Currently amended) The method of claim 60, wherein the second string includes two select transistors, wherein a first transistor in the second string and immediately adjacent to one of the two select transistors is in a desired charge storage state, wherein the program voltage is coupled sequentially to at least two selected transistors in the first string by applying sequentially the program voltage to two control gates capacitively coupled with the at least two selected transistors,

coupling a third voltage level to the first transistor in the desired charge storage state when the program voltage is applied to the two control gates, such that coupling of said third voltage level and boosting of the electrical potential(s) of the channel regions of the second string do not change the desired charge storage state of the first transistor to a different charge state, said third voltage level being less than the first ~~boosting~~ voltage level(s).

71. (Currently amended) A method for programming a memory system, said system comprising strings of charge storage transistors for storing different charge states, said strings including a first and a second string each connected between one of a

plurality of bit lines and a source line and controlled by common word lines, said method comprising:

applying a program voltage to a selected word line coupled to a selected transistor in the first string separated from the source line by at least two charge storage transistor in the first string to program the selected transistor;

coupling first ~~boosting~~ voltage level(s) to at least some of the transistors in the second string between said selected word line and the bit line connected to the second string to boost electrical potential(s) of channel regions of transistors in the second string;

coupling a voltage at or about 0 volts to at least a first one ~~of the~~ charge storage transistor in the second string between the selected word line and the source line such that a channel area of the second string on the source side of the at least first one transistor is electrically isolated from the transistor in the second string controlled by the selected word line to reduce program disturb; and

coupling second voltage level(s) that are or is less than the first voltage level(s) to at least one second charge storage transistor in the second string between the selected word line and the source line such that a channel area of the second string on the source side of the at least one second transistor coupled to the second voltage is electrically isolated from the transistor in the second string controlled by the selected word line, said second voltage level(s) including a positive voltage level.

72. – 73. (Cancelled).

74. (Previously presented) The method of claim 71, wherein the second voltage level(s) are such that it turns off the at least one transistor coupled to it or them.

75. (Original) The method of claim 74, wherein the at least one transistor that is turned off is separated from the selected word line by at least one charge storage transistor in the second string.

76. (Original) The method of claim 75, wherein a positive voltage is coupled to said at least one transistor in the second string separating the selected word line from the transistor that is turned off.

77. (Currently amended) The method of claim 76, wherein said positive voltage is in a range of about 1 to 32 volts.

78. (New) The method of claim 60, wherein said second voltage level(s) applied to the second set of transistors include(s) positive voltage levels.

79. (New) The method of claim 78, wherein one of said positive voltage levels is in a range of about 1-3 volts, and another one of said positive voltage levels is in a range of about 5-10 volts.

80. (New) The method of claim 78, wherein said positive voltage levels are in a range of about 1-3 volts.

81. (New) The method of claim 60, wherein said second voltage level(s) applied to the second set of transistors include(s) a positive voltage level and a voltage at or about 0 volts.